Modern tendencies in ASIC's development for experimental physics. ASIC's for RPC detectors.

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ASIC’s for RPC detectors.

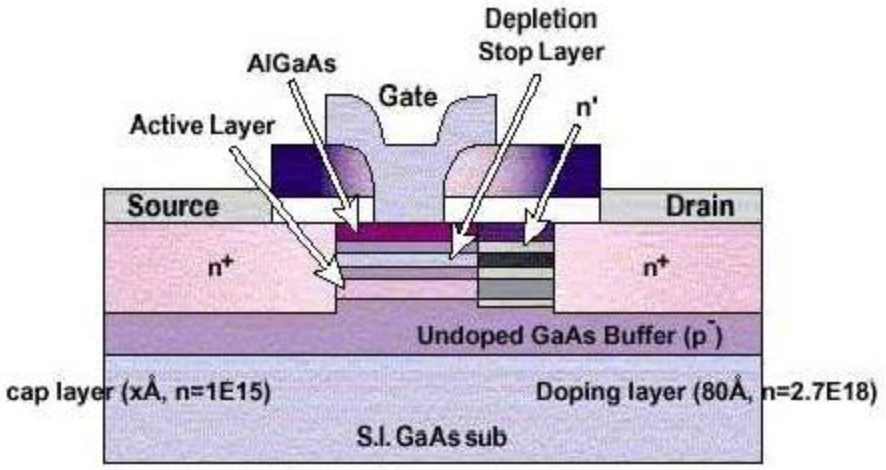
1. Introduction.
2. DIE8 ASIC for RPC muon chambers (ATLAS, CERN).
3. NINO ASIC for RPC time-of-flight chambers (ALICE, CERN).
4. PADI ASIC for RPC time-of-flight chambers (CBM, GSI).
5. Comparison and conclusion.

1. GaAs ASIC DIE8 an ultra-fast, low-power, front-end amplifier discriminator for RPC chambers in ATLAS muon system.

(1995-1997) - 0.6 μm GaAs MESFET technology - gain-bandwidth product (10^{11}). Circuit based GaAs MESFET advantages low noise transistors.

1. 8-channels of a front-end discriminator with a resulting die size of 1.5×2.3 mm ^{2}
2. A new GaAs amplifiers as voltage-sensitive input stages (voltage gain >1000),
3. Discriminator with 30-50 mV threshold level,
4. Hight sensitivity (~50 μV),
5. Fast rise time (1.5 ns) and BW -100 MHz,
1. Power consumption of 25 mW per channel.

0.6 μm GaAs MESFET advantages transistor.

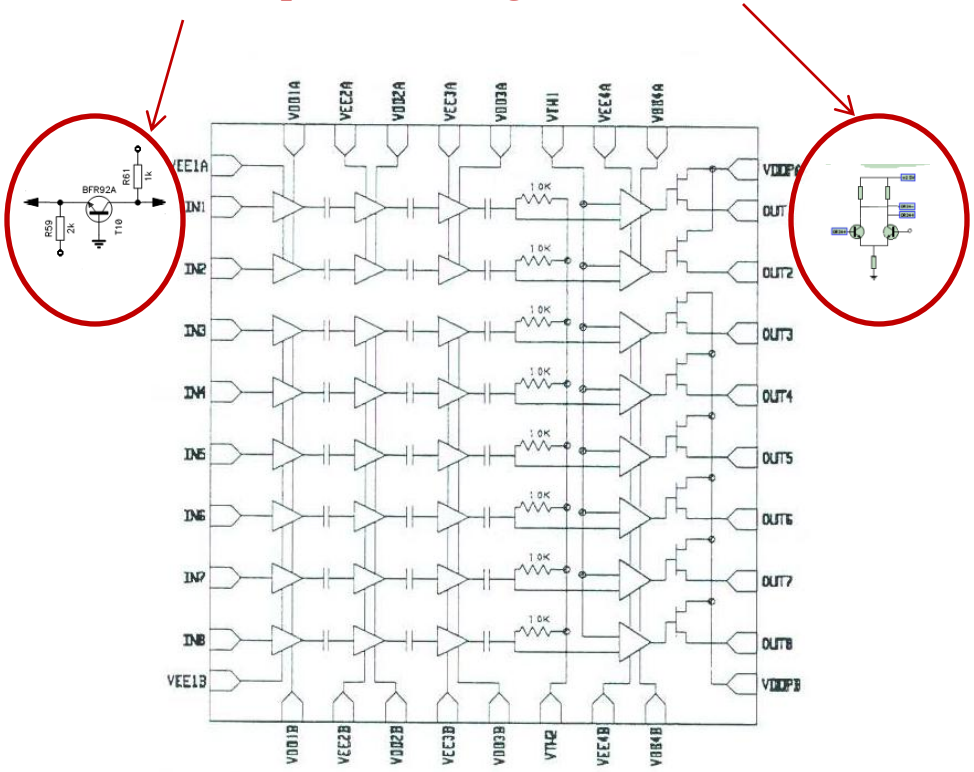


1. GaAs ASIC DIE8 an ultra-fast, low-power, front-end amplifier discriminator for RPC chambers in ATLAS muon system.

DIE8 electrical 8-channels structure

Additional external scheme

Transimpedance stage Diff. ECL driver



Problems:

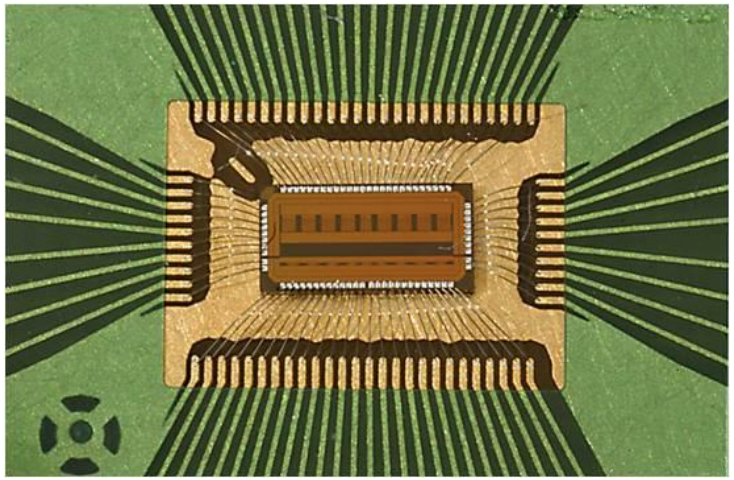
1. High impedance input 1kOhm, but 25 Ohm strip readout impedance.
2. Single ended ECL output creates pic-up interference on the inputs.
3. Minimum threshold level changed from ~50 μV to ~200 μV
4. Rise time changed from 1.5 ns to 2 ns
5. Band Width from 100 MHz to 70 MHz
6. Power consumption from 25 mW to 95mW/ channel.

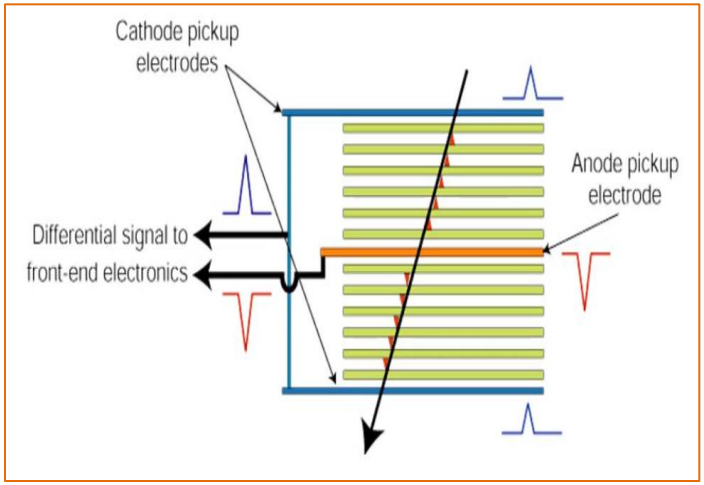
Conclusion.

1. Problem statement errors - ignore the meaning of the little things.
2. Ignoring the stages of the ASIC development process.
3. The high cost of development in an external company led to only one ASIC version.
4. The customer did not have an electronics specialist to successfully conduct work of the ASIC creation.

2. NINO, an ultra-fast, low-power, front-end amplifier discriminator for the Time-Of-Flight experiment in ALICE

DIE8 was not taken as a basis for the NINO ASIC design.





1 Specifications

1.1 Detector & related transmission line

Parameter	Value	Remark
Detector capacitance	10 pF	
Maximum signal	1.5 pC	
Signal rise time	< 200 ps	
Transmission line impedance	55 Ω	Two 110 Ω lines in parallel
Transmission line length	< 20 cm	

1.2 Front-end ASIC specifications

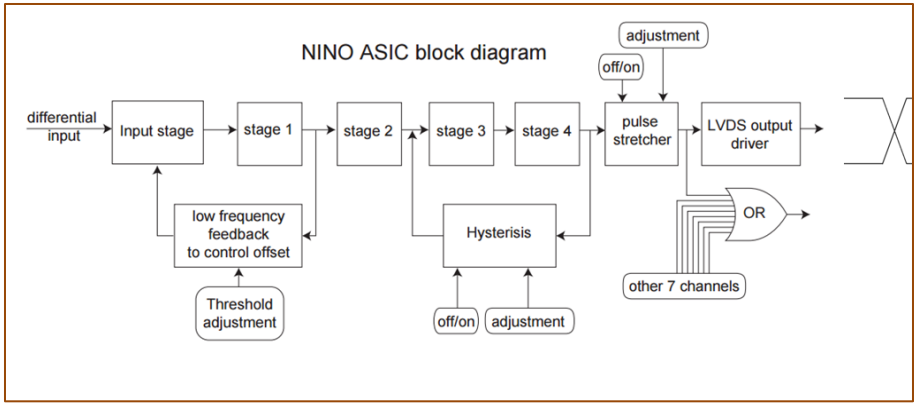
Parameter	Value	Remark
Peaking time	1 ns	1st priority spec
Linear dynamic range	0 to 100 fC	
Saturation level	> 100 fC	
Maximum signal	1.5 pC	
Noise	< 5'000 e- RMS	2nd priority spec
Jitter	< 50 ps	
Time walk	< 50 ps	
Power consumption	< 30 mW	3rd priority spec
Discriminator threshold	5 fC to 50 fC	Externally adjustable
Input impedance (differential)	55 Ω	Matched to the transmission line Zo = 55 Ω
Output interface (differential)	LVDS	User-configurable with external components

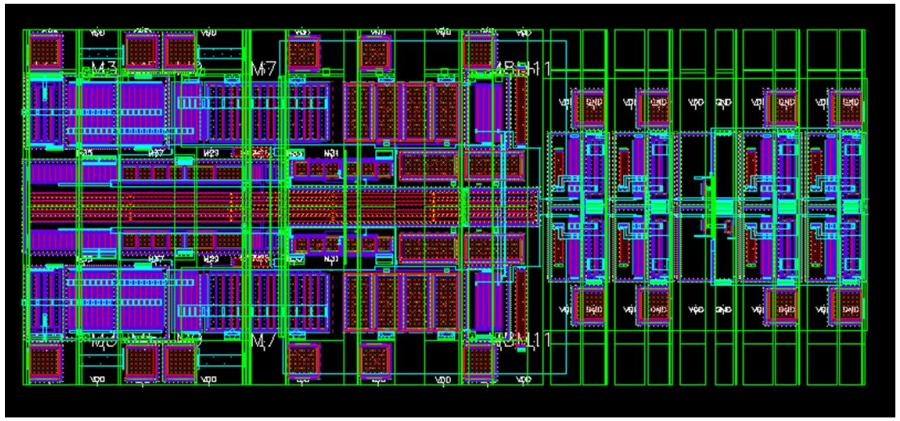
2. NINO ASIC structure and channel topology.

Almost new fully differential structure plus advanced function.

NINO ASIC specification:

- 8-channel - 2x4 mm^2 chip
- IBM CMOS 0,25um process
- 5 fC – min. threshold (60 fC – typically).
- Fully differential structure from input to output,
- Tunable input impedance (40 – 75) Ohm,
- TOT function is for amplitude analysis,
- Tunable hysteresis (0-12%),
- < 3000 el. Noise @ 10pF Cdet
- Pulse width stretcher for provide TOT function,

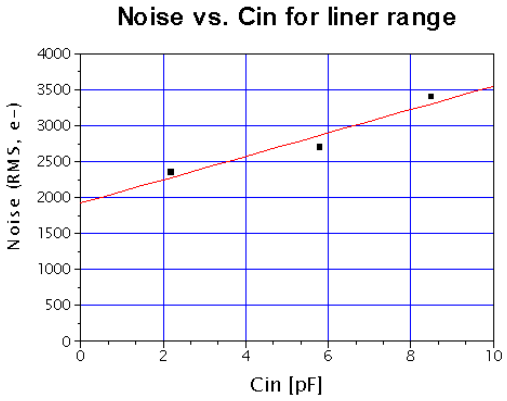




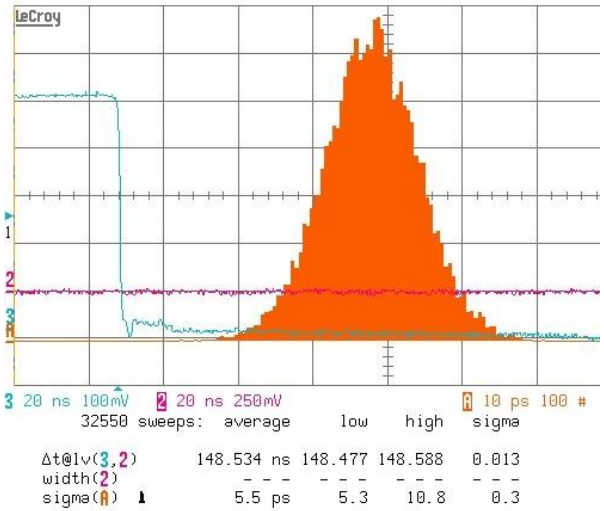
- Input stage, DC condition and Threshold setting
- Gain is obtained by 4 cascaded high bandwidth low gain stages (G=6, BW=500Mhz)

2. NINO, an ultra-fast, low-power, front-end amplifier discriminator for the Time-Of-Flight experiment in ALICE

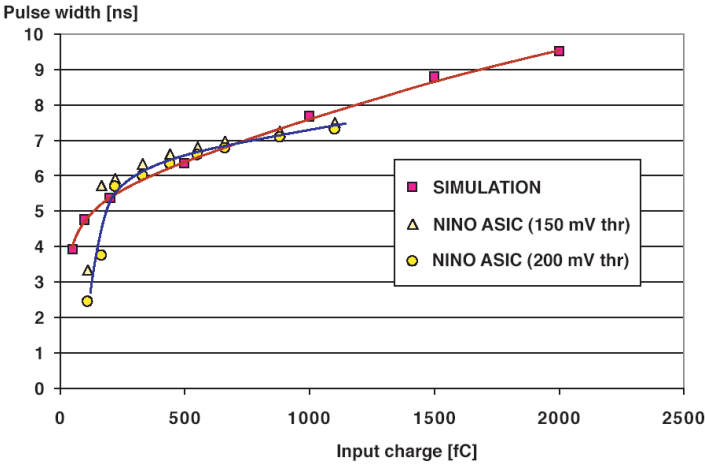
Liner regression of noise
Qnoise = 1906e- +164e- / pF



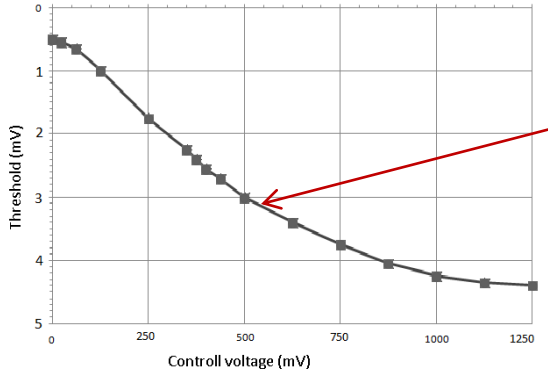
NINO jitter ~ 6ps



Pulse Width Measurement vs. Simulation

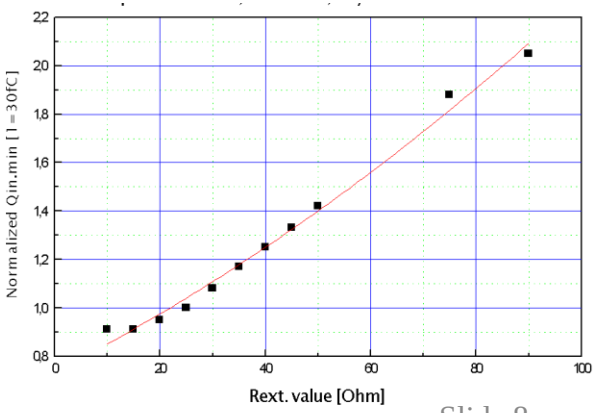


Threshold vs. control voltage is the same Transfer function



Nonlinear transfer function – especial solution for reduce hard clamping distortion in the amplification stages.

Normalized Qin vs. Rext.

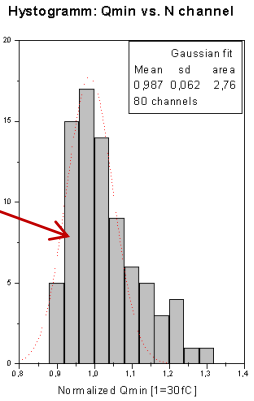


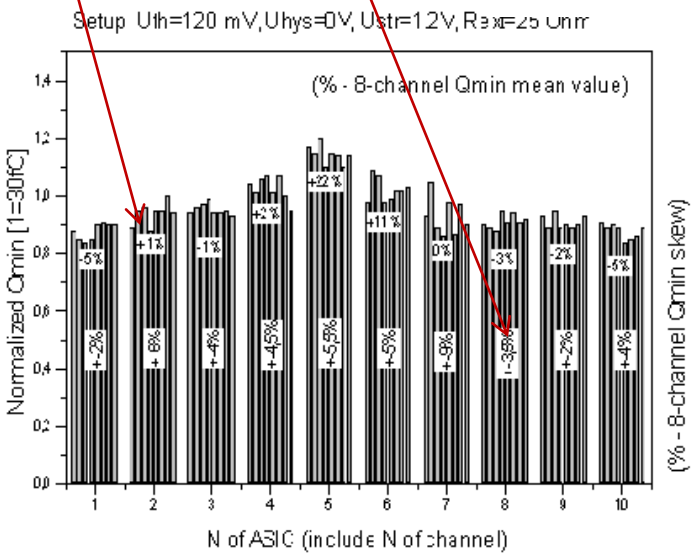
2. NINO ASIC – ELECTRICAL SPECIFICATIONS (measurements) (@ T_A=25°C, V_{dd}=+2.5V, R_{ext}=25 W)

Mass production test 10 NINO.

Threshold min. skew vs:

- number of 80 channel, 6,2%
- number of NINO, 1 by 8,
- % - inside NINO.





NINO ASIC – SPECIFICATIONS

ELECTRICAL HARACTERISTICS

(@ T_A=25°C, V_{dd}=+2.5V, Rext=25 Ω)

Parameter	Conditions	Min	Typ	Max	Unit
INPUT HARACTERISTICS:					
Input DC Offset Voltage	Rext=20, 25 ,37 Ω	0.4	0.85	1.2	V
Differential Offset Voltage			<2		mV
Threshold Levels Range (Input Charge)			10 -500		fC
Input capacitance,			1		pF
Input Differential Resistance	Rext=20, 25, 37 Ω	35	50	74	Ω
Clamping Level, Referred to Charge			>200		fC
AMPLIFICATION FACTOR:					
Input Charge To Output Voltage	Cdet=0 pF		1080		mV/fC
Input Charge To Threshold			4		mV/fC
Noise, Equivalent Charge	Ustr = 0V, Uhyst = 0V		1900 / 0.25		e / fC
Skew Of Amplification Factor			10		%
OUTPUT HARACTERISTICS:					
Output Current Brunch Range			1 - 6		mA
Stretch Timer Range	Ustr = (2.5– 0.7) V		0 - 100		ns
Typical Stretch Time	Ustr = 1.3 V		15		ns
Skew Of Stretch Time Pulse Width	Ustr = 1.3 V		10		%
Output Driver	(C-MOS dif. current branch)		LVDS compatible		
OR Output Driver	(C-MOS dif. current branch)		LVDS compatible		
DINAMIC PERFORMANCE:					
Input Small Signal Bandwidth (-3dB)			500		MHz
Rise/Fall Time			600		ps
Minimum input Pulse Width			1.6		ns
Output Pulse Width Range	Ustr = 2,5V (Q=10fC – 5pC)		1 – 6		ns
Leading Edge Jitter	Q > 200 fC		12		ps
Hysteresis Range	Uhyst = (1 – 2,5) V		0 - 12		%
POWER SUPPLY:					
Supply voltage range,		2,2	2,5	5,5	V
Supply Current One Channel		11,9	14,4	38,1	mA
Supply Current		95	115	305	mA
Power Dissipation Total			289		mW
Power Dissipation One Channel			36		mW
Power Supply Rejection Ratio			-50		dB

2. NINO, an ultra-fast, low-power, front-end amplifier discriminator for the Time-Of-Flight experiment in ALICE

Robotic test :

- 100% NINO ASICs were tested on a robotic stand,
- 97-98% chips – good,
- Robotic test checked only the DC parameters, for example, input bias voltage, output voltage levels, output pulse and supply current,
- Rejected (2-3%) chips were not checked, no analysis was performed.

2. NINO, an ultra-fast, low-power, front-end amplifier discriminator for the Time-Of-Flight experiment in ALICE

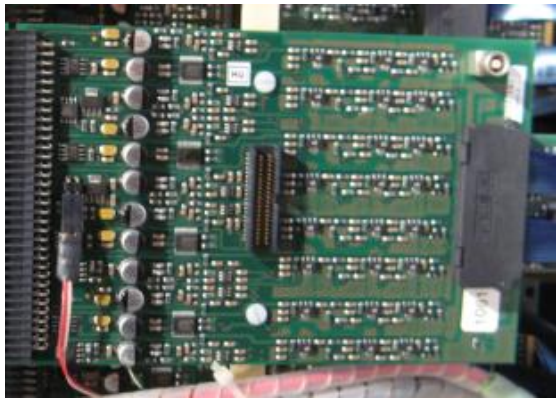
Conclusion:

- Timing jitter ~ 6 ps is main achievements of NINO ASIC design,
- Several prototypes and tests at each stage of development ensured the successful of the project,
- New additional functions (stretcher, hysteresis, TOT) have ensured the success of wide applications.
- Simple packaging and easy application of the chip for various particle detectors.

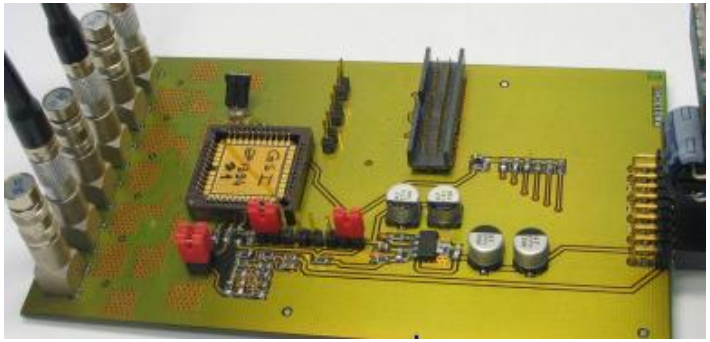
3. PADI, an ultrafast Preamplifier - Discriminator ASIC for Time-of-Flight Measurements. (CBM experiment on FAIR, GSI, Darmstadt).

PADI ASIC – is 8-channel Amplifier-Discriminator for RPC chambers.
Has been developed from 2005 to the present time.

PADI prototype - FOPI RPC FEE5



PADI ASIC – evaluation board



IEEE Transaction: «We have tested NINO and our discrete FEE5, reading out both with the FOPI acquisition system TACQUILA2 [9] and found comparable results. It became also obvious that ASICs reach lower conversion gains and less bandwidth than discrete classical layouts, for which the best available discrete integrated circuits can be selected».

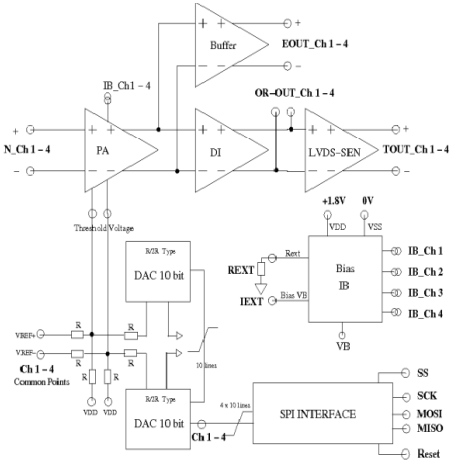
"In any case the electronics has to cope with short rise times at low amplitudes while keeping any electromagnetic pickup small; the impedance matching between FEE and electrodes should be as good as possible to minimize reflections. For the ToF system upgrade of the FOPI detector, we had designed a 16 channel preamplifier-discriminator card, FEE5. It consists of discrete elements and features a maximum gain of 220 at a bandwidth of 1.5 GHz".

3. PADI, an ultrafast Preamplifier - Discriminator ASIC for Time-of-Flight Measurements. (CBM experiment on FAIR, GSI, Darmstadt).

PADI ASIC specification:

- 8-channel chip – migrate during 15 years 0.18 μm CMOS to 0.13 μm CMOS process,
- Fully differential schem from input to output (coped NINO structure),
- Mached input impedance (30-160) Ohm,
- Additional analogue output for amplitude analysis,
- Expande amplification factor A = 250 for provide min. Thresl
- Exclude pulse strectcher - TOT function just option,

Preamplifier, line output buffer.



Voltage discriminator.

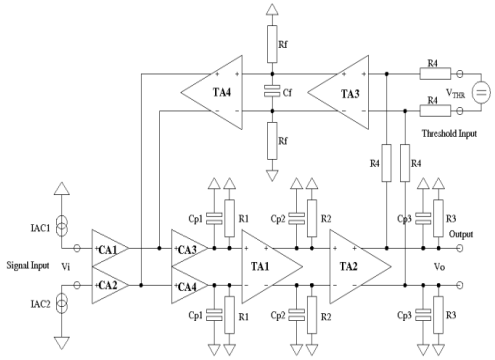


TABLE I
MAIN PARAMETERS OF THE PADI FAMILIES

Main parameters comparison	PADI-1	PADI-2	PADI-6	PADI-8
Channels per chip	3	4	4	8
PA Bandwidth (MHz)	280	293	416	411
PA Voltage Gain	74	87	244	251
Conversion Gain (mV/fC)	6.3	7.8	35	30
Baseline DC offset, σ (mV)	6.7	21.9	5.9	1
PA Noise (mV_{RMS})	3.37	2.19	5.82	5.5
Equivalent Noise Charge (e_{RMS})	3512	1753	1039	1145
Threshold type	Extern	Extern	Ext. & DAC	DAC
Threshold dynamics (+/- mV)	Non.lin. 280	Non.lin. 300	Lin 500	Lin 750
Input Impedance Range (Ω)	30 - 450	37 - 370	38 - 165	30 - 160
Power consumption (mW/channel)	21.6	17.4	17.7	17

3. PADI, an ultrafast Preamplifier - Discriminator ASIC for Time-of-Flight Measurements. (CBM experiment on FAIR, GSI, Darmstadt).

Table comparison PADI versus NINO.

Main parameters comparison	**NINO ASIC (ALICE)**	**PADI ASIC (GSI)**
Channels per chip	8	8
Conversion Gain, (mV/fC)	1080	1900
PA Bandwidth (MHz)	500	410
PA Voltage Gain, (V/V)	30	250
TOT function available	Yes	No
Stretch timer	Yes	No
Baseline DC offset, (mV)	2	1
Equivalent Noise Charge (e RMS)	1750	1150
Input Impedance Range (Ω)	35 - 75	30 - 160
Power consumption (mW/channel)	27	17
Threshold type	External	digital SPI protocol
Timing jitter (ps)	<5	<5

3. PADI, an ultrafast Preamplifier - Discriminator ASIC for Time-of-Flight Measurements. (CBM experiment on FAIR, GSI, Darmstadt).

15 years PADI development – what is the problem?

Setting of task with wrong motivation was exceed NINO parameters!

1. Global error – move prototype solutions into integrated technology.
2. Prior to the start of the design, no studies were conducted that could exclude errors in the formulation of the problem
3. Intrinsic NINO jitter < 6 ps was sloppy measured as ~80 ps!!!
4. Additional analogue output on BW 400 MHz and A=250 is a source of reflection and pick-up-noise.
5. Rising of amplification factor by preamplifier A=250 therefore of reflection and pick-up-noise too.

Conclusion.

Dangers. More then 50% ASIC's unsuccessful.

1. Conditional electronics against integration schem – principal step before design. We can't move it to IC's technology.
2. Without Prior PSPICE simulation don't possible to set task and exclude errors in the formulation of the problem.
3. Multichannel ASIC need very special individual design.
4. Each step for ASIC design must be coupled with investigations for it.

Achievements.

1. Modern ASIC's exceeded the parameters of prototypes on discrete components.
2. Only in ASIC it was possible to implement new complex functions (TOT, stretcher, hysteresis and noise compensation).
3. The experience in the PSPICE calculation allows you to combine analog and digital parts of the circuit even in highly sensitive applications.
4. Additional functions expand the application and do not increase energy consumption and cost.

References.

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4. PADI-2,-3 and -4: The second iteration of the Fast Preamplifier-Discriminator ASIC for Time-of-Flight Measurements at CBM
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